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# Detailed Behavioral Modeling of Bang-Bang Phase Detectors

Chenhui Jiang and Pietro Andreani

Ørsted-DTU, Technical University of Denmark  
Ørsted Plads building 348, Lyngby 2800, Denmark  
[cj@oersted.dtu.dk](mailto:cj@oersted.dtu.dk), [pa@oersted.dtu.dk](mailto:pa@oersted.dtu.dk)

Ulrich D. Keil

Intel Copenhagen ApS  
Mileparken 22, Skovlunde 2740, Denmark  
[ulrich.keil@intel.com](mailto:ulrich.keil@intel.com)

**Abstract**—In this paper, the metastability of current-mode logic (CML) latches and flip-flops is studied in detail. Based on the results of this analysis, a behavioral model of Bang-Bang Phase Detectors (BBPDs) is proposed, which is able to reliably capture the critical deadzone effect. The impact of jitter, and of process, voltage and temperature variations on the BBPD behavior is also investigated. The proposed model can be used with advantage in the high-level design and verification of e.g. clock and data recovery (CDR) circuits.

**Index Terms**—Bang-Bang phase detector, behavioral model, metastability, deadzone, jitter.

## I. INTRODUCTION

In modern communication systems, the demand for very large volume information transmission has increased the need for high-speed serial data receivers. In the receiver, careful design of the clock and data recovery (CDR) circuit is crucial. The CDR circuit will determine the performance of the overall transceiver system [1]. A common method to design an integrated CDR circuit involves a phase-locked loop (PLL), where a phase detector (PD) is used to detect the timing relationship between the input data and clock signal. Bang-Bang (binary) phase detectors (BBPDs) are usually employed in high-speed CDR circuits (up to 10 Gbit/s). A typical Alexander-type BBPD is shown in Fig.1 [2]. Compared to its linear counterpart, the BBPD provides simplicity in design, better phase adjustment and higher operational frequency. [3]

This paper presents the behavioral model of a 10 Gbit/s BBPD implemented in a CMOS process. Starting from a previous analysis [3], the model is extended to include relevant effects for high-speed application such as metastability and the influence of jitter. A very detailed understanding of the so-called deadzone phenomenon is demonstrated and verified by transistor-level (TL) simulations. The precise behavioral model can be exploited in system testing and verification. The model may also provide the guideline for designing CDR circuits based on the BBPD.

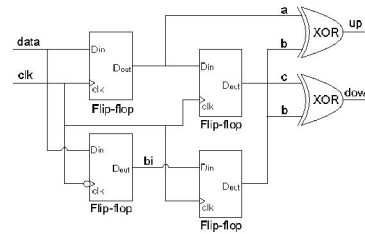


Figure 1. The Block diagram for a typical Alexander-type BBPD

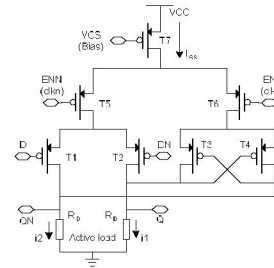


Figure 2. The CML latch with pMOS transistors

## II. METASTABILITY EFFECT IN CML CIRCUITS

### A. CML latches

The current-mode logic (CML) topology was first proposed to overcome the drawbacks existing in a conventional inverter. CML circuits can work at lower signal voltage and higher operating frequency [4]. Fig. 2 shows a CML latch with pMOS transistors. The latch has a preamplifier pair, T1 and T2, to sense and track the input data, and a regenerative pair, T3 and T4, to store the data. Two parameters,  $A_{pre}$  and  $A_{reg}$ , are introduced here to describe the slopes of the latch output in tracking and regeneration phase, respectively. They are related to the small-signal gain and the  $RC$  time constant of the latch [5]. Normally,  $A_{pre}$  is much larger than  $A_{reg}$  [3].

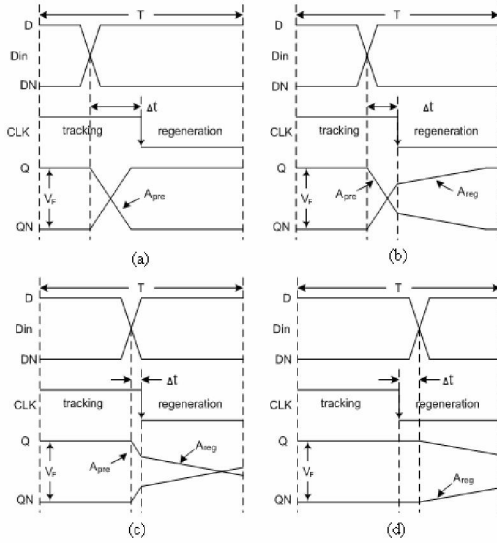


Figure 3. Four cases of CML latch behavior

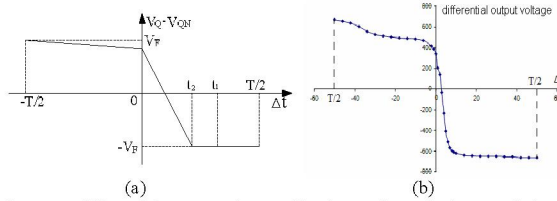


Figure 4. Differential output voltage of latches at the end of one period vs. the phase difference. (a) The characteristic from the analytical model; (b) The characteristic from transistor-level simulations. The full voltage swing is 650mV

### B. Analyzing metastability effect in CML latches

In high-speed applications, CML latches are seriously affected by metastability. The behavior of the latch based on the circuit in Fig. 2 is analyzed and presented in Fig. 3 in detail.  $\Delta t$  in Fig. 3 stands for the time difference between input data and clock signal ( $CLK$ ). It is defined to be positive if the data transition comes earlier than the corresponding falling edge of  $CLK$ , and negative if the data transition lags the  $CLK$  transition.

Fig. 3(a) shows a data transition coming so early, that the output transition is completed before the falling edge of  $CLK$  arrives. At the end of one period ( $T$ ), the differential output voltage of the latch ( $V_{out}$ ) reaches the full voltage swing  $V_F$ , equal to  $I_{SS}R_D$  ( $I_{SS}$  being the tail current and  $R_D$  the load resistance). When  $\Delta t$  becomes smaller, the transition at the output can not complete during the tracking stage. The timing point to divide those two cases is  $t_1$ , given by

$$t_1 = V_F / A_{pre} \quad (1)$$

In the regeneration stage,  $V_{out}$  can still be amplified to  $V_F$  shown in Fig. 3(b), although  $A_{reg}$  is very small. If  $\Delta t$  is small enough, as in Fig. 3(c),  $V_{out}$  can not reach  $V_F$ . The timing point,  $t_2$ , to distinguish between case (b) and case (c) is given by

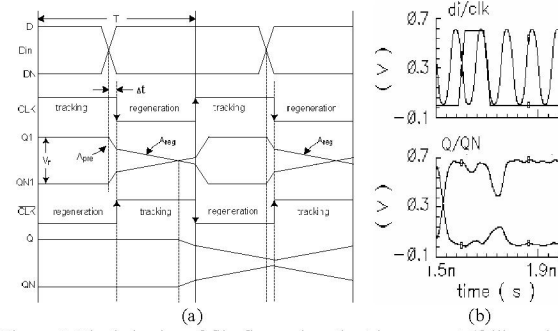


Figure 5. The behavior of flip-flops when the trigger event (falling edge of  $CLK$ ) occurs close to input data transition: (a) Analytical model; (b) Transistor level simulation. There are peaks in  $Q/QN$  presenting the single bits in data. The analytical results describe this situation precisely.

$$t_2 = (2V_F - A_{reg}T) / (2A_{pre}) \quad (2)$$

When  $\Delta t$  falls between 0 and  $t_2$ ,  $V_{out}$  is proportional to  $\Delta t$ , and is given by

$$V_{out} = (V_F - A_{reg}T) - 2A_{pre}\Delta t \quad (3)$$

$V_{out}$  is positive when  $\Delta t$  is 0, which means there is no transition event occurring at the output port in one period. When the input data transition comes later than the corresponding  $CLK$  falling edge,  $V_{out}$  only varies slightly during the regeneration stage. In this case,  $V_{out}$  is given by

$$V_{out} = (V_F - A_{reg}T) - 2A_{reg}\Delta t \quad (4)$$

The output characteristics of the latches are presented in Fig. 4. The output voltage does not have the ideal binary character because of the latch metastability. There is a finite slope for small values of  $\Delta t$ . When the time difference is negative, the output voltage varies slightly with respect to the phase difference. When the time difference is larger than  $t_2$ , the output voltage stays constant at full voltage swing. The characteristics of the CML latch obtained with both the analytical model and the TL simulation match well.

### C. Analyzing metastability effect of flip-flops

Flip-flops are key components in typical Alexander-type BBPDs. The performance of the BBPD heavily relies on the operation of flip-flops. A flip-flop is composed of two latches in a master-slave configuration. Based on the analytical model of latches, the behavior of flip-flops can also be considered analytically, as shown in Fig. 5(a). In Fig. 5(a), the input data can be read as "101". Because the trigger events of  $CLK$  are in the vicinity of data transitions, the flip-flop can not sample the input data correctly. There are some peaks presenting residual "0" in the output. This behavior is verified with TL simulation. Fig. 5(b) shows that some single bits will be lost in the output, when trigger events are closed to data transitions. In this case, only short peaks are present at the output in place of the single-bit transitions, exactly as predicted by the analytical model. This comparison shows that the analytical model is reliable. These peaks would be filtered out by subsequent limiting buffers and flip-flops.

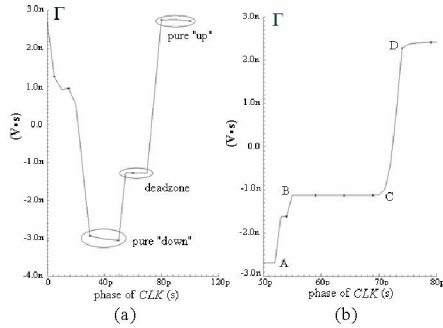


Figure 6. Characteristic of BBPDs ( $\Gamma$ ) from TL simulation: (a) Overall view; (b) Details for the deadzone region.

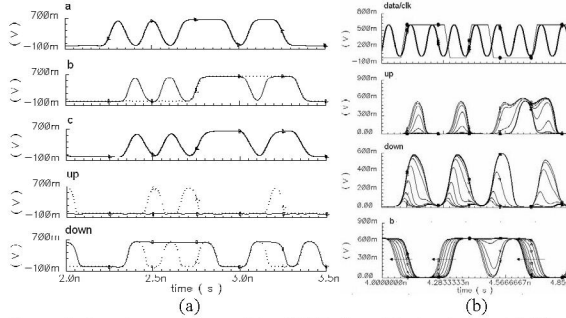


Figure 7. Transient response of the BBPD from TL simulation: (a) When the BBPD operates outside of the deadzone (solid line), all the samples are consistent with input data (and here only “down” signals are generated). When BBPDs work in the second part of the deadzone (dashed line), “b” sample loses single bits. Some solid “down” bits are replaced by dashed “up” bits, corresponding to the lost bits in “b”. (b) BBPDs work in the third part of the deadzone. The phase of  $CLK$  sweeps from “C” to “D” denoted in Fig. 6(b). The time step is 0.4ps.

### III. DEADZONE MODEL OF BANG-BANG PHASE DETECTOR

#### A. Analysis of BBPD's deadzone property

In order to evaluate the performance of BBPDs, a new parameter,  $\Gamma$ , is defined as below:

$$\Gamma = \int V(up)dt - \int V(down)dt \quad (5)$$

where  $V(up)$  and  $V(down)$  are the output voltages of BBPDs.  $\Gamma$  is the difference of the integrals of “up” and “down” in arbitrary time duration. It represents the characteristic of BBPDs. This definition is developed according to the operation of the charge pump and the loop filter following the BBPD in the phase locked loop. The value of  $\Gamma$  depends on the input data pattern and the integration interval. Only the shape of  $\Gamma$  is of interest here. This consideration will be applied to all the following figures about  $\Gamma$ . Ideally,  $\Gamma$  should be a monotonic, two-valued function.

TL simulations are implemented to obtain the BBPD characteristic at room temperature when the bit rate is 10Gbit/s. Fig. 6(a) shows the overall view of the BBPD characteristic, where the X-axis shows the initial phase of  $CLK$ . The phase is relative to the time difference between data and  $CLK$  because the phase of data is fixed during the simulation. The BBPD characteristic is not ideal, since there is an intermediate part between the top and the bottom values.

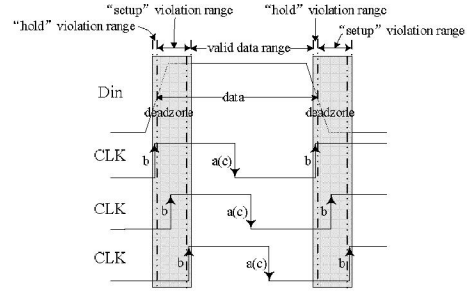


Figure 8. Behavior of BBPDs in single “1” case. “a” and “c” are sampled at the falling edging of  $CLK$ . “b” is sampled at the rising edging of  $CLK$ . The gray rectangles denote the deadzone divided into 3 parts by dashed line. The first part of the deadzone is called “hold” violation range and the second and third parts together are called “setup” violation range. The data can only be sampled definitely in the “valid data range”.

This section is referred to as “deadzone”, where the phase detector provides no gain. Its existence results from metastability effects in the flip-flops composing the BBPDs.

The details of the deadzone region are illustrated in Fig. 6(b). The deadzone section is divided into 3 parts by the limit points A, B, C, and D in Fig. 6(b). In the major part of the deadzone, between B and C,  $\Gamma$  is constant and negative. The transient response of the BBPD in this case is shown in Fig. 7(a). The “a”, “b”, and “c” signals are corresponding to the samples denoted in Fig. 1. The solid lines denote the signals when the BBPD operates outside of the deadzone. The samples contain all bits in the input data. When the BBPD operates in the deadzone, the “b” sample loses single bits in the input data, shown as a dashed line. The bit absence is caused by mentioned metastability in flip-flops. Because of the absence of single bits in “b”, some bits in the “down” signal are replaced by “up” signals. The output of the BBPD alternates between “up” and “down”, and a deadzone is generated. In the first part of the deadzone, the “b” sample loses single bits gradually. In the third part of the deadzone, the lost bits in “b” are recovered gradually, and “b” shifts from synchronization with “c” to synchronization with “a”. The transient response in this case is shown in Fig. 7(b).

#### B. The behavioral model of BBPDs with deadzone effect

When the  $CLK$  trigger takes place near the data transition, metastability will prevent the flip-flops in BBPDs to sample single bits in the input data correctly. Such an undefined sampling operation causes the deadzone phenomenon in the characteristic of BBPDs.

Fig. 8 shows the analytical model of the BBPD behavior, based on a deadzone with three different regions. The first part is regarded as the “hold” violation range, because it is located right before the next data transition. The second and third parts together are called “setup” violation range, because they are located right after the data transition. Fig. 8 shows the case when a single “1” is sampled by the BBPD. When “b” falls into the “hold” violation range, the single “1” is not stable to satisfy the “hold time” condition. The corresponding output depends on the previous input data pattern. When “b” enters the second part of the deadzone, the “setup time” condition is not fulfilled for a well-defined



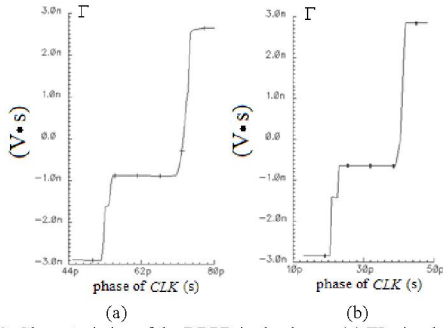


Figure 9. Characteristics of the BBPD in deadzone: (a) TL simulation; (b) Behavioral-level simulation

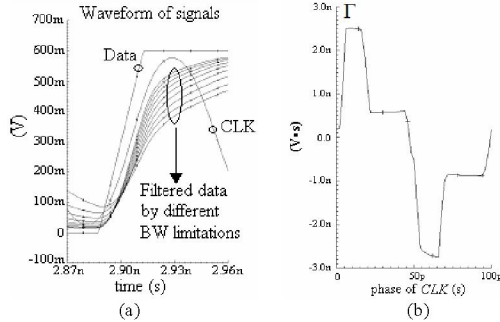


Figure 10. (a) Waveforms of  $CLK$ , ideal data and filtered data caused by the BW limitations; (b) Characteristic of the BBPD with the BW limitation

sampling, and the output of “b” is determined by the previous output. It should be noticed that the data sampled at “b” is synchronized with “c” although some single bits are lost. When “b” sampling moves out of the deadzone, “b” sample is the same as “a” sample. The “lost bits” of “b” caused by metastability are recovered at the end of the “setup time”.

From the TL simulations results, a BBPD behavioral model can be developed in Verilog-A. As shown Fig. 9, BBPD characteristics simulated with both the TL and the behavioral model are almost identical. Thus, we can conclude that our behavioral model is capable to accurately capture the BBPD behavior in the deadzone as well.

#### IV. JITTER EFFECT

ISI jitter greatly affects the BBPD performance. It has two causes. The first is the bandwidth (BW) limitation of the BBPD, mainly determined by the input impedance of the BBPD and the output impedance of the block driving the BBPD. As shown in Fig. 10(a), a limited BW results in a signal with reduced amplitude and delayed phase. This data distortion affects the characteristic of the BBPD, whose deadzone becomes larger, as shown in Fig. 10(b).

TABLE I. DATA PATTERN CATEGORIES

Input data pattern	X000→1	X100→1	X010→1	X110→1
Normalized starting values for transitions	0	0.02	0.13	0.15

The values of starting points for data transitions are calculated based on 3GHz BW limitation and normalized to full voltage swing of the data. In the data pattern, “X” indicates arbitrary value of the bit and the arrow indicates the transition of interesting.

The other source of ISI jitter is the input data pattern itself. Because of the mentioned BW limitation, data-dependent exponential transients will not, in general, have fully decayed when the next bit arrives at the input, which means that the same input data will result in slightly different zero crossings, dependently on the previous data pattern.

Based on analyzing values of starting points for data transitions with a 3GHz BW limitation theoretically, all data patterns can be fit into four categories after ignoring small variation resulted from different data patterns. The normalized starting values to the full voltage swing corresponding to different data patterns are listed in table 1.

#### V. PROCESS, VOLTAGE AND TEMPERATURE VARIATION

Since BBPDs are designed in CMOS processes, their performance is influenced by process, bias voltage and temperature variation. If the process is faster, the deadzone will be smaller. If the bias voltage is increased or the temperature is reduced, the range of the deadzone will be decreased. The smallest deadzone is observed with the BBPD with a fast process and typical at lower temperature and higher bias voltage.

#### VI. CONCLUSION

The behavior of BBPDs in high-speed applications is analyzed in detail. The behavioral model of BBPDs is developed including high-speed effects. The model is successfully verified against TL simulations. When the behavioral model replaces the TL model of the BBPD in transient simulations, the simulation time is decreased by more than ten times.

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